IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Geeng-Chuan Chern

Application No. 09/916,618

Filed: July 26, 2001

For: SELF ALIGNED METHOD OF FORMING A SEMICONDUCTOR MEMORY ARRAY OF FLOATING GATE MEMORY CELLS WITH VERTICAL CONTROL GATE SIDEWALLS AND INSULATION SPACERS, AND A MEMORY ARRAY MADE THEREBY

Group Art Unit: Unknown

Examiner: Unknown

PRELIMINARY AMENDMENT

1755 Embarcadero Road
Palo Alto, CA 94303-3340
(650) 833-2000

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, Washington, DC 20231, on Dec. 4, 2001.

GRAY CARY WARE & FREIDENRICH Date 12/4/01

By: Kathleen LaBrie

Kathleen LaBrie

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please preliminarily amend the above identified application as follows:

I. CLEAN VERSION OF AMENDED PARAGRAPHS

Please substitute the following paragraph for the corresponding paragraph specified from the specification:

Paragraph on page 2, lines 1-13:

In the split-gate architecture, the memory cells can be formed in mirrored pairs. Figure 1A illustrates a partially formed pair of memory cells, with floating gates 1 disposed over a substrate 2. A source region 3 is formed in the substrate 2, and is electrically connected to a